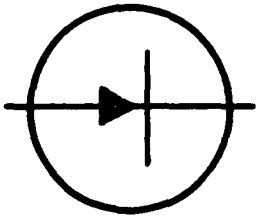
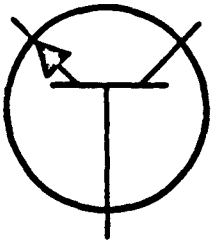
Westinghouse

ELECTRIC CORPORATION





(5) WESTINGHOUSE ELECTRIC CORP[redacted]

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Washington, D. C.

(9) [redacted] Quarterly Report. no. 5, 1 Aug-31 Oct 64.

[redacted]

(6) 500 WATT SILICON POWER TRANSISTOR.

(15) Contract NObsr-91001, Proj. [redacted] SR-0080304, Task [redacted] 9347

(16) Navy Department
Bureau of Ships
Electronics Division (17)

fdc

TABLE OF CONTENTS

ABSTRACT

Results of secondary-breakdown tests are discussed and development of a power gain test is reported. The triple-diffusion fabrication process is described. Details of the encapsulation structure and characteristics are presented.

1. INTRODUCTION

Testing of several transistor types has established limits of critical energy for secondary breakdown in the unclamped inductive mode. A fast crowbar circuit to make this test nondestructive is under development. Safe operating conditions in the clamped inductive test were also established. The power gain test circuit has been developed.

The complete triple-diffusion fabrication process has been established, and some results have been obtained. Additional details, including production experience in the encapsulation, have been accumulated.

2. PERSONNEL

Engineering time as follows was charged to the subject contract in the fifth quarter:

M. F. Amsterdam	---	288
V. Balodis	---	356
R. F. Chick	---	36
T. E. Ebert	---	232
H. E. Ferree	---	250
R. A. Forrest	---	348
D. V. Gennaro	---	4
T. G. Stehney	---	284
P. A. Trongo	---	40

A total of 1,838 hours of technician time was charged to the contract.

3. FACTUAL

3.1 Electrical Testing for Second Breakdown

The second breakdown study described in the previous quarterly reports was continued. Construction of the permanently-packaged test circuit was completed and some time was devoted to troubleshooting and optimizing this circuit. The remainder of the period was spent in gaining experience with the tester and in accumulating data on some of our standard commercial transistors.

3.1.1 Testing Program: Thus far, three different types of Westinghouse alloy transistors have been used for investigation -- Types 108, 115 and 118. The testing was performed by the clamped and unclamped inductive turn-off methods as described in the previous reports. The results of all testing performed to date are summarized below.

TABLE I: Unclamped Inductive Circuit

Device	Max. Rating	Critical Energy for Second Breakdown	
108D	200V, 7.5A	45 to 870 mj.	at I_c = 7.5A
115D	200V, 30A	42 to 170 mj.	at I_c = 25A
115F	300V, 30A	60 to 180 mj.	at I_c = 25A

It is interesting to note that the minimum critical energy for second breakdown is almost the same for the 115 transistor (two emitter rings) as for the 108 transistor (one emitter ring), despite their different maximum ratings. One possible explanation for this seeming paradox is that the localized nature of the second breakdown phenomenon (current crowding, hot-spots) makes it relatively independent of junction area.

TABLE II: Clamped Inductive Circuit

Device	Max. Rating	Safe Conditions for Inductive (Rectangular) Switching Load Line
108D	200V, 7.5A	I_c = 7.5A, V_{CE} = 200V, T_c = 100°C, f = 400cps
115D	200V, 30A	I_c = 30A, V_{CE} = 200V, T_c = 110°C, f = 2400cps
118D	200V, 10A	I_c = 10A, V_{CE} = 200V, T_c = 110°C, f = 1200cps

It should be noted that the data obtained in Table I were obtained by discharging the entire inductive stored energy into the transistor at a very low repetition rate (two pulses per second). The energy per discharge was slowly increased until second breakdown and, consequently, destruction of the transistor occurred.

However, in the case of the clamped imductive data of Table II, most of the inductive energy is dissipated in the clamping circuit, rather than in the transistor. The repetition rate and the case temperature were therefore greatly increased in an attempt to show second breakdown. Each set of safe conditions represents the results of 15-minute runs of at least ten transistors. These tests were performed during the period of circuit optimization which was necessary to permit the higher frequency operation. The data of Table II should therefore not be interpreted as critical conditions for second breakdown, since this phenomenon was never observed in the clamped testing mode. The differences in repetition rate were simply imposed by circuit limitations at the time the tests were being made, or by switching speed in the case of the 118.

The only conclusion to be drawn from Table II, therefore, is that these particular types and voltage classes of alloy transistors are capable of operating in a rectangular switching path which passes through the point

of maximum rated collector-emitter voltage and maximum rated collector current at a high repetition rate without experiencing second breakdown, provided that the collector voltage is clamped to the rated maximum value.

3.1.2 Circuit Development: The experience gained during the last period again made evident the disadvantages of this destructive method of second breakdown testing. It is often desirable to test for second breakdown under a wide variety of conditions. When only a small number of transistor samples is available, this is obviously impossible. Also, if reasonably good accuracy is desired, human errors cannot be tolerated and the testing becomes quite tedious.

Our efforts to make the testing nondestructive were therefore redoubled. The most profitable design approach appears to be a fast crowbar circuit which will operate in less than one microsecond after the onset of second breakdown. This circuit will be shunted across the device under test and when triggered, will place a low impedance short circuit across the device diverting the current from the device until a conventional circuit-breaker can open.

A trigger circuit using fast switching transistors has been designed and is being constructed. Owing to the three possible modes of operation of the main second breakdown circuit (see previous quarterly reports) it was necessary to provide two possible sources of trigger signal.

a. The circuit will trigger on a negative dV/dt of collector-emitter voltage for the forward base-emitter bias mode.
b. The circuit will trigger on a "burst" of damped V_{BE} oscillation which occurs at second breakdown for the two reverse base-emitter bias modes (clamped and unclamped V_{CE}).

Since low stray inductance and capacitance is important in the construction of this circuit, it could not be built and checked out in breadboard form and is therefore being constructed on a chassis using the best known

high-frequency techniques. When completed, it should provide a powerful tool for the gathering of second breakdown data.

3.2 Other Electrical Evaluation

A circuit has been designed and constructed for measuring the power gain of the subject device. The power gain of a transistor operating in a push-pull Class B circuit may be expressed as follows:

$$\text{Power Gain} = \frac{I_C^2 R_L^1}{I_B^2 h_{ie}}$$

where I_C and I_B are the rms values of the collector and base currents and R_L^1 and h_{ie} are the load resistance seen by each transistor and the input resistance of each transistor, respectively. In large signal amplifiers, this expression is complicated by the nonlinearity of h_{ie}. In this test, the assumptions are made that all voltages and currents are sinusoidal so that measurements may be made oscillographically at the crest of the various waves. The following expression may then be written for power gain:

$$\text{Power Gain} = \frac{I_{C\ pk} V_{O\ pk}}{I_{B\ pk} V_{IN\ pk}}$$

where $V_{O\ pk}$ is the peak value of the A-C component of load voltage seen by each transistor during its conduction and $V_{IN\ pk}$ is the corresponding peak value of V_{BE}.

The circuit is shown in Figure 3.2.1. The drive circuit, an emitter follower, provides a low impedance driving source which gives a more linear transfer characteristic (I_C vs. V_{BE}) than does a high impedance source (I_C vs. I_B), and consequently, gives relatively low distoration in the output. The low impedance drive results in slightly pessimistic values for power gain owing to the distortion in the base current wave.

The power gain test will be operated under the following conditions:

Supply voltage = 250VDC
$V_{CE\ pk}$ = 500VDC
$I_{C\ pk}$ = 8A

These conditions will produce a peak collector dissipation of 500 watts.

3.3 Device Fabrication

The process used in the fabrication of the all-diffused device has been modified in some aspects from that outlined in the last report. Those areas undergoing marked changes were slice preparation and metalization. These changes will be discussed in more detail in the following section, which deals in more depth with the actual processes.

The silicon wafers used for this device are 5.4-5.5 mils thick, P-type, with a bulk resistivity of 200 ohm-cm. As received, the wafers are lapped on both sides (Figure 1). After a thorough solvent cleaning, they are subjected to lengthy acid soakings which remove all organic and inorganic contaminants. The wafers are then oxidized on both sides (oxide thickness = 10-12K Å). The oxide is then stripped from one side and the wafers are polished in an HCl vapor etch. The resulting wafer is shown in Figure 2 . The oxide protects the silicon from the etch, thus just one side of the wafer is polished. The reason for this polishing is to prepare a surface on which a uniform, nonporous oxide can be grown. This oxide will then be used to mask this side of the silicon from a subsequent diffusion cycle. However, the oxide grown prior to the HCl vapor etch has been found to be lacking in that some etching has resulted on the side which was to be protected by the oxide. Just as the oxide grown on lapped surfaces is not of sufficient quality to protect against a diffusion, so it has been found lacking in protecting against the HCl vapor. The problem of preparing a polish surface is a major process problem and causes much delay. Other approaches from different angles are being investigated:

a. Attempts will be made to grow thicker, less porous oxides on the original lapped surfaces prior to HCl etch.
b. Some slices will be mechanically polished on one side.
c. Some slices will be chemically polished on one side.

After one surface of the wafer is polished, the wafers are oxidized (Figure 3) on both sides.

Using HF, the oxide is stripped from the lapped surface. Onto this surface a P^+ base region is deposited from a liquid BBr_3 source. This is shown in Figure 4. This P^+ base region is then driven into the wafter (in an open-tube furnace at 1250°C) to a predetermined depth. Figure 5 is a drawing of the cross section showing this step.

After completion of the P^+ drive, the oxide is stripped from both sides of the wafer. A phosphorus deposit is then made from a phosphorus source. Figure 6 illustrates this step. The wafers are then coated with Kodak metal etch resist. The desired emitter geometry is defined in the resist by aligning a photographic mask properly with respect to the wafer. All masks (both emitter and subsequent contact masks) have been produced in the Youngwood facility which has been established to supply quality 2" x 2" masks. After aligning the mask with the coated wafer, the two are brought into contact, and the resist is polymerized by exposing the unmasked areas to a beam of ultraviolet light. The unpolymerized resist is then dissolved in the appropriate solvents. The remaining resist is thoroughly inspected for edge definition, pinholes in the resist image, and unremoved resist. All wafers that have an acceptable image defined on them are placed in an air oven to harden the image prior to the etch cycle.

The next step is to remove the unwanted N^+ impurity area and thus define the emitter geometry in the wafer. Since the N^+ region must not be removed from the collector side, this area is protected from the subsequent silicon

etch by coating it with an acid-resistant wax. Thus, the collector side is protected from the etch by wax and the emitter area is protected by the photo resist. The slices are then etched in an HF-HNO_3-HAc etch to a depth greater than the X_j of the N^+ impurity (Figure 7).

After a thorough solvent cleaning to remove all KMER and wax, the slices are diffused to a depth which will give the desired base width for the transistor (Figure 8).

After this diffusion, the gold contacts are evaporated on the device. Unwanted gold (that atop the emitter periphery) is then removed by etching the metal with aqua regia. Prior to this, of course, the contact mask must be accurately aligned and exposed. Again KMER is used to protect areas which are to remain unetched.

Previously, silver contacts were tried; but the results, both physical and and electrical, were very discouraging. The silver contacts were found to be undercut and ragged. Electrically, the units tested were found to be shorted. It appeared that the dissolved silver replated on the junction and shorted the units. No such adverse effects resulted from using gold contacts.

The actual devices were then contoured and etched. Units made by the triple-diffusion process, with the structural parameters given in Table III, were found to have collector-emitter voltage ratings of 350 volts. Reverse junction characteristics are shown in Figures 9 , 10 and 11 , and Figure 12 displays the low-voltage collector-emitter leakage. The breakdown characteristics of the devices were generally good, but gain was considerably lower than the objective of 10 at 10 amperes. The poor gain is believed to be partly due to unsufficiently slow cooling after the final diffusion step, and this will be corrected in future runs.

TABLE III

X_{j1}	= 38.9 microns	$C_1 = 8 \times 10^{19}$ atoms/cm^3
X_{j2}	= 50.8 microns	$C_2 = 2.6 \times 10^{18}$ atoms/cm^3
X_{j3}	= 42.2 microns	$C_3 = 2 \times 10^{20}$ atoms/cm^3
W_b	= 50.8 microns	$C_B = 6.5 \times 10^{13}$ atoms/cm^3

3.4 Encapsulation

The encapsulation design remains essentially the same as described in the previous report. Some experience has been gained by using the external capsule parts for a thyristor device which is now in production.

3.4.1 Capsule Modifications: A minor change was made in the steel hexagonal part called the "Integral Case-Weld Ring." To reduce weight, for better appearance and for jigging convenience, the upper .25" of this part was turned down to a cylindrical cross section, leaving the hex nut .38" high. Figure 13 shows the new outline of the Type 145 device as compared to the standard Type 200 device.

3.4.2 Thermal Impedance: An estimate of junction to case thermal impedance required (θ_{J-C} = .2°C/watt) and an estimate of the impedance expected (θ_{J-C} = .111 °C/watt) in the tentative capsule design were given in the third quarterly report of this contract.

The westinghouse Type 220 thyristor which is now in production uses the same external capsule as the tentative Type 145 capsule. Production experience to date indicates a typical θ_{J-C} = .1°C/watt. The maximum acceptable value is θ_{J-C} = .13°C/watt. These values confirm the previous estimate.

It should be noted that the thyristor device has a lower junction temperature (about 125°C) and lower heat dissipation than is expected from the 500 watt Type 145 transistor.

The operating conditions specified for the Type 145 transistor are very severe and the feasibility of using a threaded heat sink possibly with water cooling should be considered. If the device is mounted in the conventional manner in a clearance hole in the heat sink, the case to sink thermal impedance can be expected to be about .1°C/watt. This would result in a temperature drop of 50°C. With a threaded heat sink, this

might be reduced to 30°C. θ_{J-C} for the device should also decrease by about 30% because of the utilization of this additional heat transfer path.

3.4.3 Structural Strength: This subject was also discussed in the third report. Further investigation into the strength of the tellurium-copper base leads to the conclusion that the strength of the present design should be quite sufficient even at 200°C. The creep strength for annealed tellurium copper is listed as 8500psi for .1% extension in 1000hr.* Also confidence is gained from long experience with silicon rectifiers such as the Westinghouse Type 339 operating at a rated junction temperature of 190°C and storage temperature to 200°C.

3.4.4 Internal Structure: The internal structure remains essentially as given in the third quarterly report to the extent that it was described. Some evaluation remains to be done to determine which of several possible methods is best for application of pressure to the top surface of the device. Several types of insulating washers are possible; but for first samples, a high alumina ceramic washer will be used. Below this washer, a layer of cushioning material will prevent stress concentrations in the silicon.

The current carrying requirements are small enough that the leads should cause no space or assembly problems.

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* "Chase Copper Alloy Handbook," 9th Edition, Sept. 1, 1960; "Standards Handbook Copper and Copper Alloys," 5th Edition, Copper Development Association.

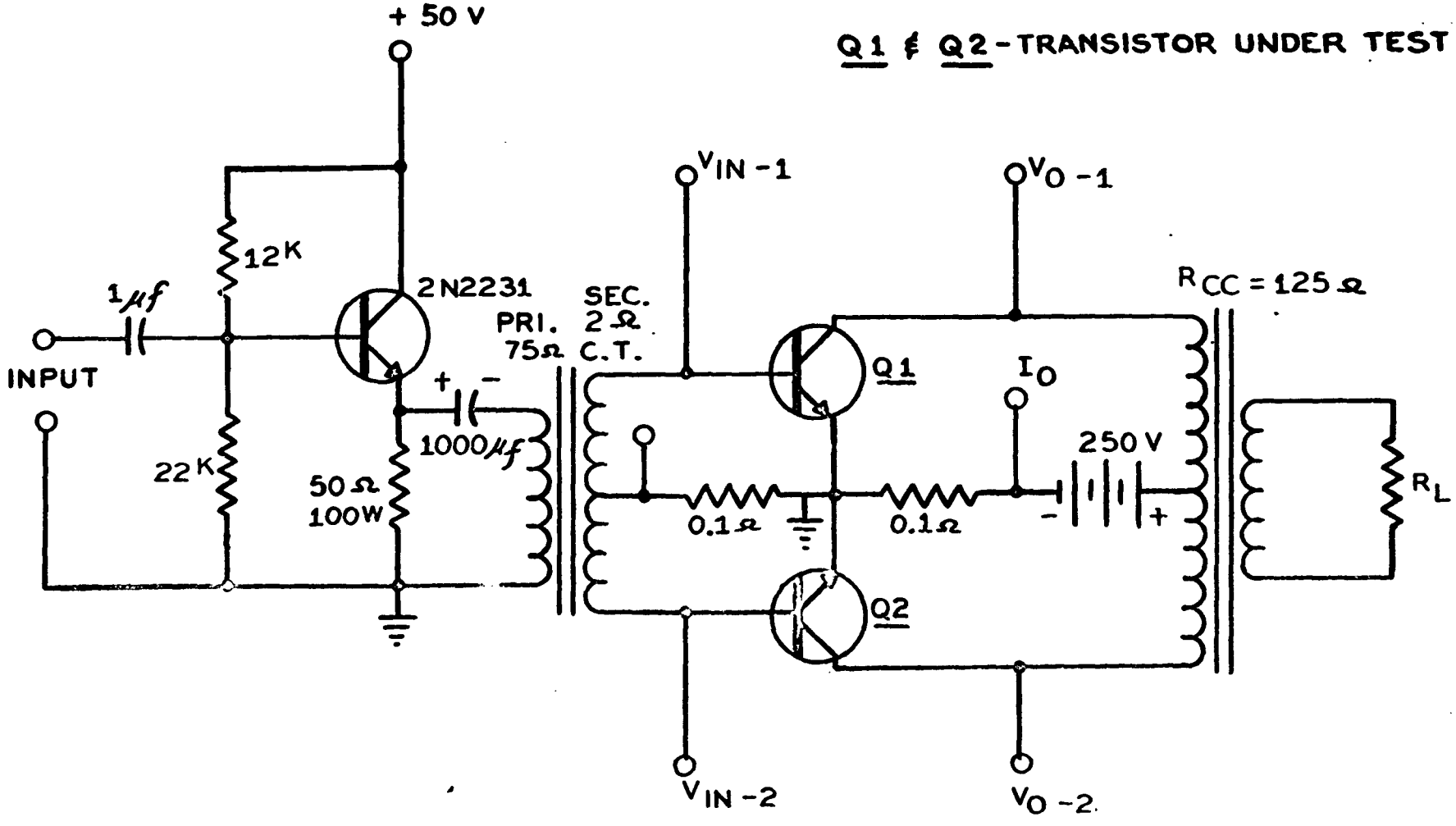
4. CONCLUSIONS

The development of the testing methods had been completed and tests were made. Process improvements were continued while design samples were being fabricated and evaluated. The process, however, should not be considered as final; further refinement is necessary. Although the initial samples did not confirm to the objectives, they clearly indicated the feasibility. The thermal characteristics of the encapsulation were shown to be adequate for the subject device.

5. PROGRAM FOR NEXT QUARTER

The next quarter will be a crucial period for process refinement and design finalization. State-of-the-art samples will be fabricated.

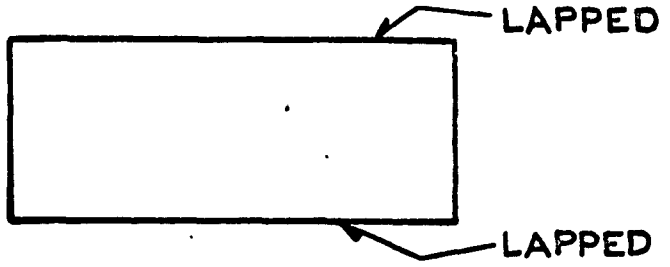
6. ILLUSTRATIONS



$$\text{POWER GAIN} = \frac{P_{OUT}}{P_{IN}} \cong \frac{V_{OPK}\, I_{O\,PK}}{V_{IN\,PK}\, I_{IN\,PK}}$$

FIG.- 1-A

POWER GAIN TEST



THICKNESS = 5.4 - 5.5 MILS.
P TYPE 200 Ω cm

FIG. - 1 STARTING WAFER

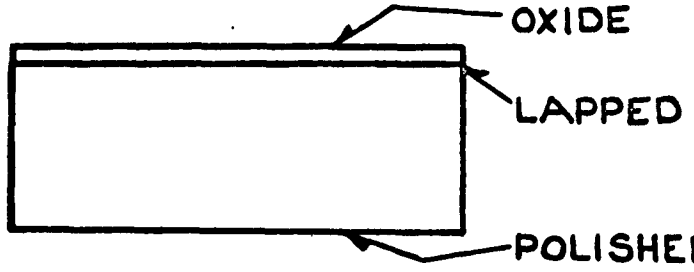


FIG. - 2 POLISHED WAFER (AFTER HCL VAPOR ETCH)

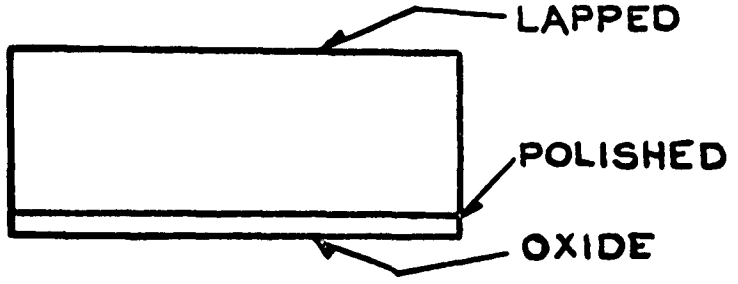


FIG. - 3 WAFER PRIOR TO P^+ DEPOSIT

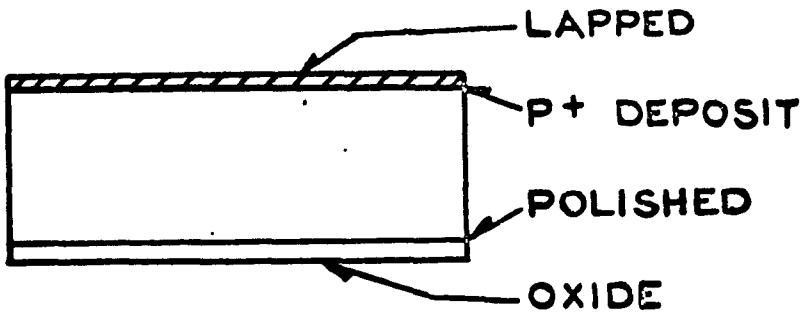


FIG.-4 P+ DEPOSITED WAFER

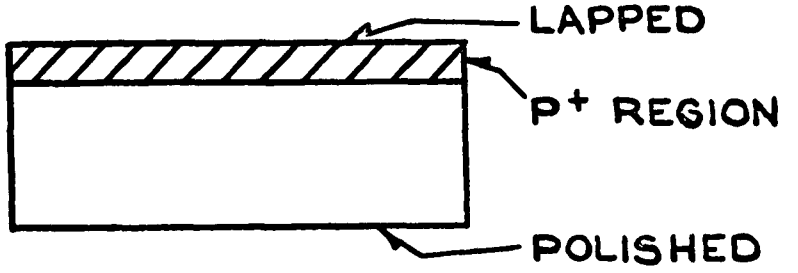


FIG.-5 P+ REGION DRIVEN INTO WAFER

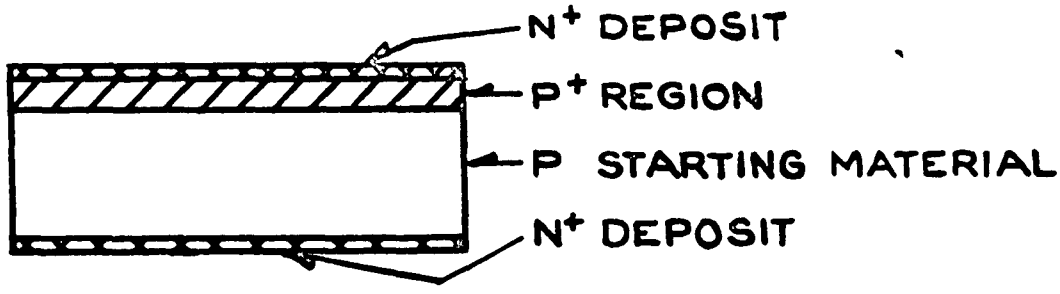


FIG.-6 WAFER WITH N+ DEPOSITS

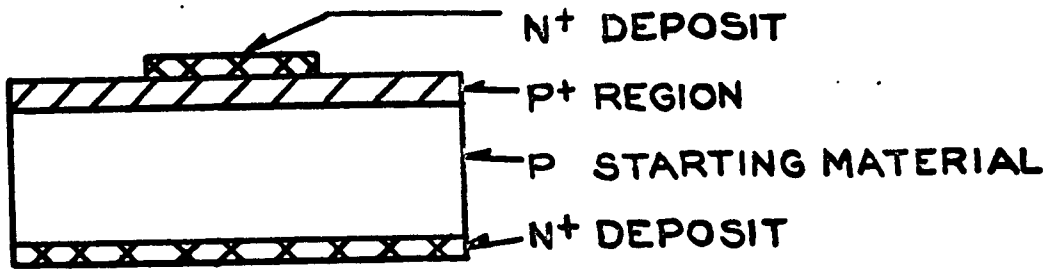


FIG.-7 WAFER AFTER EMITTER MASKING AND SILICON ETCH

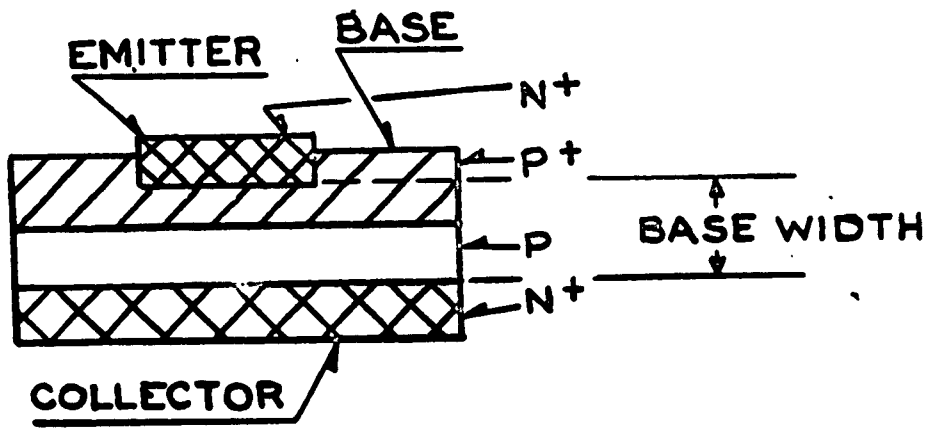


FIG.-8 FINAL DEVICE

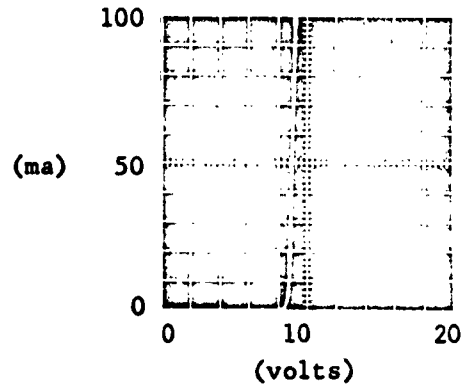


FIGURE 9: BV_{EBO} Horizontal: 2V/div. Vertical: 10ma/div.

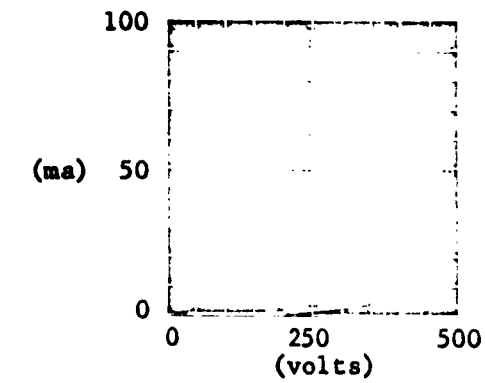


FIGURE 10: BV_{CBO} Horizontal: 50V/div. Vertical: 10ma/div.

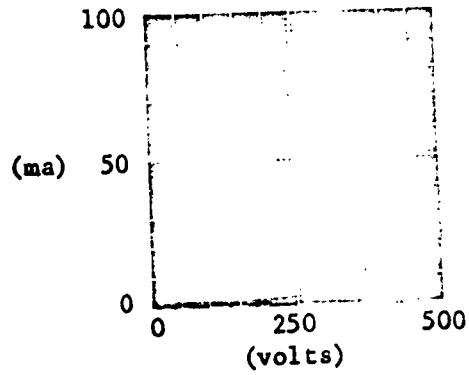


FIGURE 11: BV_{CEO} Horizontal: 50V/div. Vertical: 10ma/div.

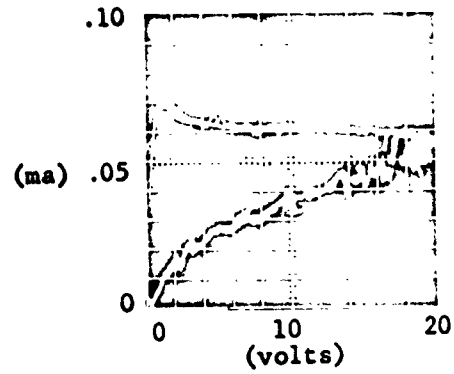


FIGURE 12: I_{CEO} Horizontal: 2V/div. Vertical: 0.01ma/div.

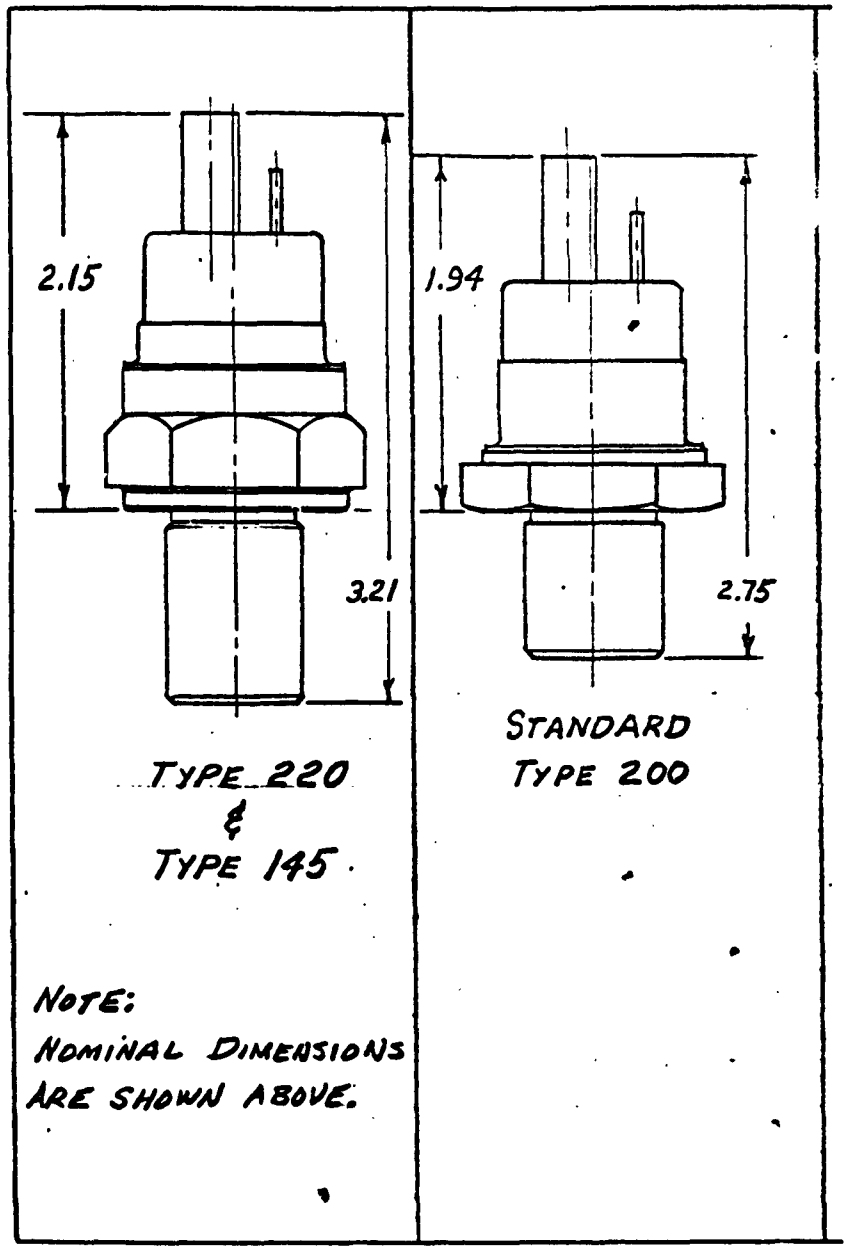

2.15
3.21
TYPE 220
&
TYPE 145
1.94
2.75
STANDARD
TYPE 200
NOTE:
NOMINAL DIMENSIONS
ARE SHOWN ABOVE.

FIGURE 13